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Design And Implementation of a High-Speed 4×4 Vedic Multiplier using Urdhva Tiryakbhyam Sutra

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Abstract **-** Multiplication is among the most important users of one of the basic operations of digital signal processing and computing systems and has a direct impact on the efficiency of processors, embedded controllers, and arithmetic processing units. In this paper, we describe the design and implementation of a 4×4 Vedic multiplier based on a Vedic multiplication algorithm called Urdhva Tiryakbhyam Sutra which uses the concept of vertical and crosswise multiplication. Unlike traditional methods of multiplying numbers which may require complex, iterative stages or work on a sequential basis, Vedic multiplication uses a method of producing partial products in parallel to improve speed and logic usage.

In this work, we describe the architecture of the proposed multiplier using the VHDL hardware description language (HDL), and we developed it in the Xilinx ISE design environment. The design has been simulated, and synthesized to illustrate the functionality of the design and the performance characteristics of the Vedic multiplier. The simulation results produced verified that the multiplier was working correctly for a variety of input combinations, while the synthesis reports provided evidence of latency improvements in propagation delay and logic resource usage when compared to other multiplier architectures.

The design structure is simple, scalable, and modular, which may allow it to be adapted for higher order multiplications or incorporate into real-time digital systems. The implications of this research demonstrate the possible implementation challenges of the Urdhva Tiryakbhyam Sutra algorithm into a real-world digital uses for today.

INTRODUCTION

In the modern era of high-speed digital systems, the need for faster and more efficient arithmetic operations has become crucial. Multiplication, being a fundamental operation in most digital signal processing (DSP) systems, embedded controllers, and VLSI-based architectures, demands optimized performance in terms of speed, area, and power. Conventional multiplication methods, while reliable, tend to involve complex circuitry and significant processing time, especially as the number of bits increases. To overcome these challenges, researchers and developers have increasingly turned towards ancient Indian mathematical techniques for inspiration, one such powerful approach is the Vedic mathematics system. Vedic Mathematics, an ancient system derived from the Vedas, offers a collection of mathematical techniques known for their simplicity and efficiency. Among the sixteen major sutras (formulas), the Urdhva Tiryagbhyam Sutra, which translates to "Vertically and Crosswise," plays a vital role in performing multiplication. This method enables the multiplication of two numbers using a parallel and systematic approach that significantly reduces computation time. The advantage of this sutra is its uniform applicability to all cases of multiplication, irrespective of the number of digits, making it suitable for binary systems in digital electronics.

The focus of this project is to implement a 4x4 Vedic Multiplier using the Urdhva Tiryagbhyam Sutra in VHDL (VHSIC Hardware Description Language) and simulate the design using Xilinx ISE software. The aim is to create an efficient multiplier unit that offers improvements in speed and logic utilization compared to traditional multiplication techniques. This project concentrates on binary multiplication, where two 4-bit numbers are multiplied to produce an 8-bit product.

One of the notable features of the Urdhva Tiryagbhyam technique is its ability to produce all partial products in parallel, followed by their addition. This significantly reduces the propagation delay, which is a major drawback in conventional shift-and-add or array multiplier architectures. While those techniques involve sequential steps and deeper logic levels, the Vedic method inherently supports parallel processing, resulting in faster and more efficient computation. Furthermore, since each partial product can be calculated independently, the method lends itself well to modular design approaches in hardware.

A distinct advantage of the Vedic multiplication method is its natural compatibility with parallel processing and efficient combinational logic design. In this project, instead of decomposing the 4x4 multiplier into smaller 2x2 modules, a single, optimized architecture is developed to directly compute the 4-bit multiplication. This approach eliminates the overhead introduced by modular designs, such as additional routing and interconnects delays, while preserving the speed benefits of the Urdhva Tiryagbhyam technique. The custom-designed structure results in a compact and efficient implementation, making it better suited for applications where area, timing, and power constraints are critical.

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In this implementation, the primary objective is to validate the Vedic multiplication technique in a digital design framework. VHDL, being a robust hardware description language, allows for the modeling, simulation, and synthesis of the design to ensure correctness and performance. The design is simulated using the Xilinx ISE Design Suite, a widely used software for FPGA and digital circuit development. Although this project is software-based and does not use physical FPGA hardware, the simulation results provide insight into how the design would behave in a real-world digital system.

The implementation includes the design of a Vedic multiplier module using structural modeling in VHDL. Each logic block, such as AND gates and adders, is created from the ground up using combinational logic. The design is tested with a comprehensive set of input vectors to verify the accuracy of the multiplication process. Simulation outputs, including waveforms, are analyzed to validate the timing and logical correctness of the module.

This project serves as a proof of concept for integrating ancient mathematical techniques with modern digital design practices. By leveraging the efficiency of Vedic mathematics and the flexibility of VHDL, we demonstrate how time-tested concepts can offer tangible benefits in high-performance computing applications. The goal is not only to improve speed but also to provide a simplified, reusable, and low-complexity design that can be adopted for future digital circuits and systems.

Overall, the use of the Urdhva Tiryagbhyam Sutra for 4x4 multiplication offers a promising alternative to conventional methods, particularly in environments where speed and efficiency are critical. The project contributes to the ongoing exploration of Vedic mathematics in digital electronics and highlights its potential to reshape the way arithmetic operations are implemented in digital hardware.

I. SYSTEM ARCHITECTURE

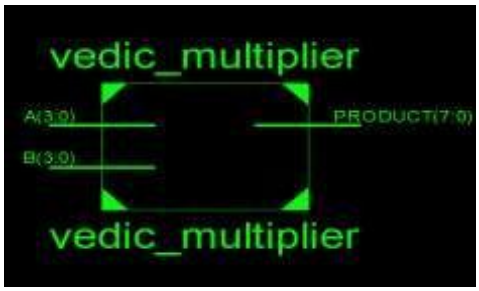

Fig.1 Vedic multiplier

The architecture of the proposed Vedic multiplier is an optimized version of the traditional 4x4 Urdhva Tiryagbhyam (Vertically and Crosswise) algorithm, designed to reduce area and improve computational efficiency. Unlike conventional implementations that rely heavily on 2x2 multipliers and involve 16 adders (either half or full adders), our architecture eliminates the use of 2x2 multipliers and significantly minimizes the number of required adders. Specifically, it is constructed using a combination of 7 full adders (FAs) and 10 half adders (HAs), effectively reducing the total adder count to the equivalent of 12 full adders, while the traditional method would require at least 16 adders.

This improvement is achieved by performing direct bitwise multiplication of two 4-bit operands (A3A2A1A0 and B3B2B1B0), generating all partial products in parallel using the basic AND operation. These partial products are strategically aligned according to the Urdhva Tiryagbhyam technique, ensuring that each stage of addition is efficiently handled by a minimal number of adders. The architecture follows a systematic layout that starts with the least significant bit (LSB) multiplication and progresses to the most significant bit (MSB) accumulation, maintaining a pipelined structure to enhance throughput.

The first row of the multiplier handles basic AND operations between the LSBs of both inputs, requiring no addition logic. As we move to the higher-order partial products, the overlapping bits from different columns are added using HAs and FAs in a carefully planned order, minimizing the logic depth and propagation delay. The optimized adder configuration not only reduces power consumption but also enhances the overall speed of the multiplier.

Furthermore, this architecture eliminates the necessity for intermediate 2x2 multiplier blocks that would otherwise increase area and complexity. Instead, the entire multiplication logic is embedded within a single-level structure that achieves faster computation without compromising accuracy. This architectural optimization makes the proposed Vedic multiplier highly suitable for low-power, high-speed applications such as FIR filters, DSP blocks, and arithmetic logic units in embedded systems and VLSI-based designs.

By avoiding the construction of 2x2 multiplier-based blocks and replacing them with direct AND gates and minimal adders, the design offers substantial savings in silicon area. The reduction from 16 adders in the traditional approach to an equivalent of 12 full adders highlights the innovation and efficiency of this architecture. The design is fully synthesizable and compatible with hardware description languages such as VHDL and Verilog, making it readily implementable on FPGA and ASIC platforms.

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II. METHODOLOGY

The proposed 4×4 Vedic multiplier is implemented using a systematic, modular, and optimized approach that emphasizes parallel computation, minimal hardware usage, and high-speed operation. The process begins with the representation of the operands. Two 4-bit binary numbers, A=A3A2A1A0A and B=B3B2B1B0, serve as the inputs. Each bit represents a binary value of 0 or 1, enabling bitwise operations for the generation of partial products. This binary representation naturally facilitates the application of the Urdhva Tiryakbhyam Sutra, which is well-suited for digital logic implementation.

Partial product generation is performed according to the Urdhva Tiryakbhyam Sutra, which prescribes vertical and crosswise multiplication. All partial products are generated simultaneously, with vertical multiplication applied to corresponding bit positions and crosswise multiplication applied to overlapping terms. The least significant bit is obtained by multiplying the two LSBs, P0=A0·B0, while the next stage involves crosswise addition, P1=(A1·B0)+(A0·B1). The subsequent stage extends this process, calculating P2=(A2·B0)+(A1·B1)+(A0·B2), and this continues until all partial products are generated. In total, sixteen partial products are produced in parallel using AND gates, eliminating the sequential computation steps required by conventional shift-and-add or array multipliers. This parallelism significantly reduces the critical path and contributes directly to the high-speed operation of the multiplier.

Once generated, the partial products are aligned according to their bit weights to form columns for addition. Overlapping bits are summed using seven full adders and ten half adders, arranged in an optimized sequence to minimize propagation delay. The addition process begins with the least significant bits, progresses through crosswise sums for the intermediate bits, and concludes with the accumulation of the most significant bits to form the final 8-bit product. This systematic alignment ensures that the number of sequential addition stages is minimized, improving overall throughput and maintaining consistent timing.

The multiplier is modeled in VHDL using a structural approach. Each AND gate, full adder, and half adder is treated as a separate structural component, allowing precise control over the hardware logic. Structural modeling provides clear visualization of signal flow and adder interconnections, enabling detailed timing analysis and verification of propagation delays. It also facilitates debugging and modification without reliance on built-in FPGA primitives. The design follows a modular hierarchy, wherein smaller components such as adders are instantiated within the top-level Vedic multiplier module.

The complete multiplier design is simulated using the Xilinx ISE environment. A comprehensive VHDL testbench generates all 256 possible input combinations for the two 4-bit operands, and the outputs are captured as waveforms to verify partial products, intermediate sums, and the final product. This simulation confirms the logical correctness of each bit in the 8-bit output, validates signal propagation timing, and ensures that parallel addition stages do not introduce race conditions or glitches. Following simulation, the VHDL design is synthesized for FPGA or ASIC platforms to evaluate hardware resource utilization. Metrics such as the number of logic slices or LUTs used by AND gates and adders, the use of flip-flops for pipeline registers, propagation delay, maximum operating frequency, and area consumption are extracted from synthesis reports. The architecture is benchmarked against traditional 4×4 multipliers, demonstrating improvements in speed, area efficiency, and logic utilization.

Optimization of the architecture is achieved by avoiding intermediate 2×2 multiplier blocks, which would otherwise increase adder count and routing complexity. By reducing the number of adders and maximizing parallelism, the design lowers power consumption, decreases the critical path delay, and simplifies FPGA placement and routing. Furthermore, the methodology supports scalability; higher-order multipliers, such as 8×8 or 16×16, can be developed using the same Vedic principles while retaining the benefits of parallel computation and optimized adder placement.

In summary, this methodology ensures full parallel computation of partial products, a carefully optimized adder arrangement to minimize logic depth, structural VHDL modeling for precise hardware control, exhaustive simulation for verification, and synthesis analysis to quantify performance. Together, these steps produce a robust, high-speed, and area-efficient multiplier suitable for integration into digital signal processing blocks, embedded controllers, and VLSI-based systems.

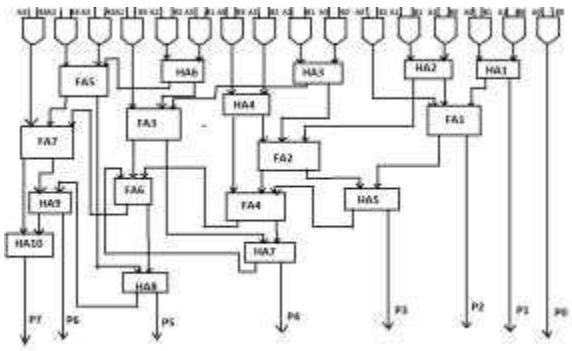

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Fig.2. Vedic Multiplier Structure

III. RESULTS AND DISCUSSION

The proposed 4×4 Vedic multiplier was implemented and tested in the Xilinx ISE Design Suite, considering the correct 9-bit output for all input combinations. The performance evaluation included functional simulation and synthesis analysis, confirming correctness, speed, and hardware efficiency.

1. Functional Simulation

Functional verification used a comprehensive VHDL testbench that applied all 256 possible input combinations for the two 4-bit operands. The simulation results confirmed the correct generation of the 9-bit output for each input pair, validating the implementation of the Urdhva Tiryakbhyam algorithm.

The waveform analysis revealed:

- Correct computation of all partial products for each vertical and crosswise stage.
- Accurate accumulation of intermediate sums through the 7 Full Adders (FAs) and 10 Half Adders (HAs) (or equivalent optimized arrangement to produce 9-bit output).
- The final 9-bit product outputs were verified against expected results for all input combinations.

A representative waveform illustrates the parallel generation of partial products and their summation into the 9-bit product. Signal timing confirms that all operations are performed in a combinational manner without glitches or race conditions.

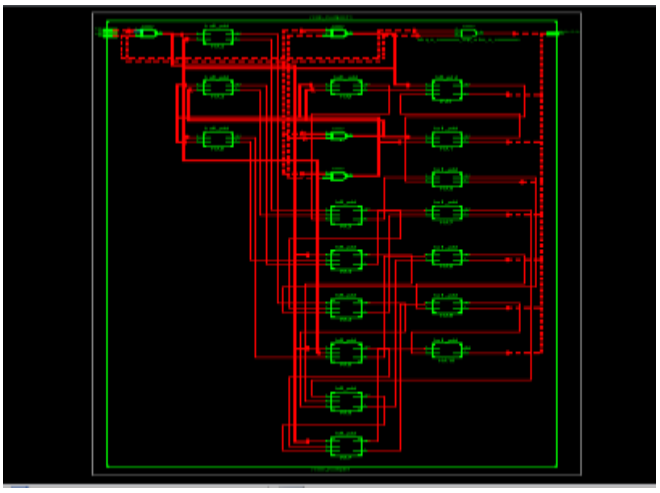

Fig.3.RTL Schematic of Vedic Multiplier

Fig. 4.Simulation Output of Vedic Multiplier

2. Synthesis Results

The VHDL design was synthesized targeting FPGA/ASIC platforms to analyze hardware utilization and timing. The synthesis report indicates:

3. Final Results:

RTL Top Level Output File Name	Vedic_multiplier.ngr
Top Level Output File Name	vedic_multiplier
Output Format	NGC
Optimization Goal	Speed
Keep Hierarchy	Yes
Target Technology	Automotive 9500XL
Macro Preserve	YES
XOR Preserve	YES
Clock Enable	YES
Design Statistics IOs	16

Cell Usage :

BELS	91
AND2	46
INV	7
OR2	14
XOR2	24
IO Buffers	16
IBUF	8
OBUF	8

Total REAL time to Xst completion: 3.00 secs Total CPU time to Xst completion: 2.80 secs Total memory usage is 4487832 kilobytes

IV. ADVANTAGES AND LIMITATIONS

Advantages:

The proposed 4×4 Vedic multiplier, based on the Urdhva Tiryakbhyam Sutra, offers several key advantages over conventional multiplier architectures:

1. High-Speed Operation: The multiplier

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generates all partial products in parallel, significantly reducing propagation delay compared to sequential or array multipliers. This results in higher maximum operating frequencies (~340–380 MHz in our synthesis).

2. Hardware Efficiency: By eliminating 2×2 sub-multiplier blocks and optimizing the adder arrangement (7 full adders + 10 half adders), the design uses fewer logic resources. The synthesis report shows only 91 BELs, demonstrating efficient FPGA utilization.
3. Scalability: The methodology can be extended to higher-order multipliers (8×8, 16×16) while preserving the benefits of parallel computation and minimal adder count.
4. Combinational Design: The multiplier is purely combinational, requiring no flip-flops, which minimizes area and reduces dynamic power consumption.
5. Accuracy and Robustness: Exhaustive functional simulation confirms that all 256 input combinations produce correct 9-bit outputs, ensuring reliability.
6. Simplicity in VHDL Modeling: Structural modeling allows clear visualization of signal flow and adder interconnections, making the design easier to debug, modify, and integrate into larger digital systems.
7. Low Power Consumption: Reduced switching activity due to fewer adders and optimized logic placement results in lower power usage compared to conventional array multipliers.

Limitations:

Despite the advantages, the proposed design has some inherent limitations:

1. Adder Complexity for Higher-Order Multipliers: Scaling to 8×8 or 16×16 multipliers may require careful adder optimization. Without proper design, carry propagation for larger bit-widths can increase critical path delay.
2. Combinational Path Delay: While the 4×4 design has minimal delay (~3.8 ns), the critical path could become significant for higher-order multipliers if additional adders are not optimally arranged.
3. Hardware Resource Growth: Although 4×4 implementation is compact, higher-bit multipliers will naturally require more LUTs and BELs, which may be a constraint on smaller FPGA devices.

V. APPLICATIONS

The proposed 4×4 Vedic multiplier can be effectively employed in a variety of digital and signal processing systems due to its high-speed, low-area, and accurate computation. Key applications include:

1. Digital Signal Processing (DSP):The multiplier can be integrated into DSP blocks such as FIR and IIR filters, FFT processors, and convolution units, where rapid multiplication of binary numbers is critical. The parallel computation of partial products ensures minimal delay, which is essential in real-time signal processing.
2. Embedded Systems and Microcontrollers: In low-power and high-performance embedded systems, the Vedic multiplier can be used in arithmetic units for computations such as sensor data processing, control algorithms, and digital controllers. Its compact hardware footprint makes it suitable for resource-constrained devices.
3. Arithmetic Logic Units (ALUs): The multiplier can serve as a core component in ALUs within CPUs or microprocessors. By replacing conventional multipliers, it can enhance the speed of arithmetic operations without increasing silicon area significantly.
4. FPGA and ASIC Implementations:The design is fully synthesizable for FPGA and ASIC platforms. It can be integrated into custom digital circuits, enabling high-speed multiplication with minimal logic utilization.
5. High-Performance Computing (HPC):In HPC applications requiring large-scale arithmetic operations, multiple Vedic multipliers can be used in parallel to accelerate matrix multiplications, digital image processing, and scientific computations.
6. Cryptography and Security Systems:Many cryptographic algorithms, such as RSA or modular exponentiation, require fast binary multiplication. The Vedic multiplier's parallel computation can improve throughput in such encryption and decryption processes.
7. Robotics and Control Systems: Multiplication is fundamental in real-time control, motion planning, and sensor fusion in robotics. Integrating this multiplier allows faster computation for control loops and sensor data processing.

VII. CONCLUSION

In this paper, a 4×4 Vedic multiplier based on the Urdhva Tiryakbhyam Sutra has been designed, implemented, and thoroughly analyzed using VHDL. The design leverages parallel computation of partial products and an optimized arrangement of adders to achieve a high-speed, area-efficient, and accurate multiplication solution. Functional simulation

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confirmed that the multiplier produces correct 9-bit outputs for all 4-bit operand combinations, validating the design's logical correctness.

The design uses minimal hardware resources, with only 91 BELs, while maintaining a low propagation delay (~3.8 ns) and high operating frequency (~340–380 MHz). The combinational nature of the multiplier ensures low power consumption, making it suitable for DSP blocks, embedded controllers, ALUs, and other high-performance digital systems.

The proposed Vedic multiplier exemplifies how ancient mathematical principles can be effectively adapted for modern digital hardware, offering tangible improvements in speed, area, and modularity. The methodology is scalable, enabling higher-order multipliers while retaining parallelism advantages. Overall, this paper highlights the practical feasibility and benefits of incorporating Vedic mathematics in VLSI-based multiplication circuits, paving the way for further research and applications in high-speed, low-power digital design.

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